

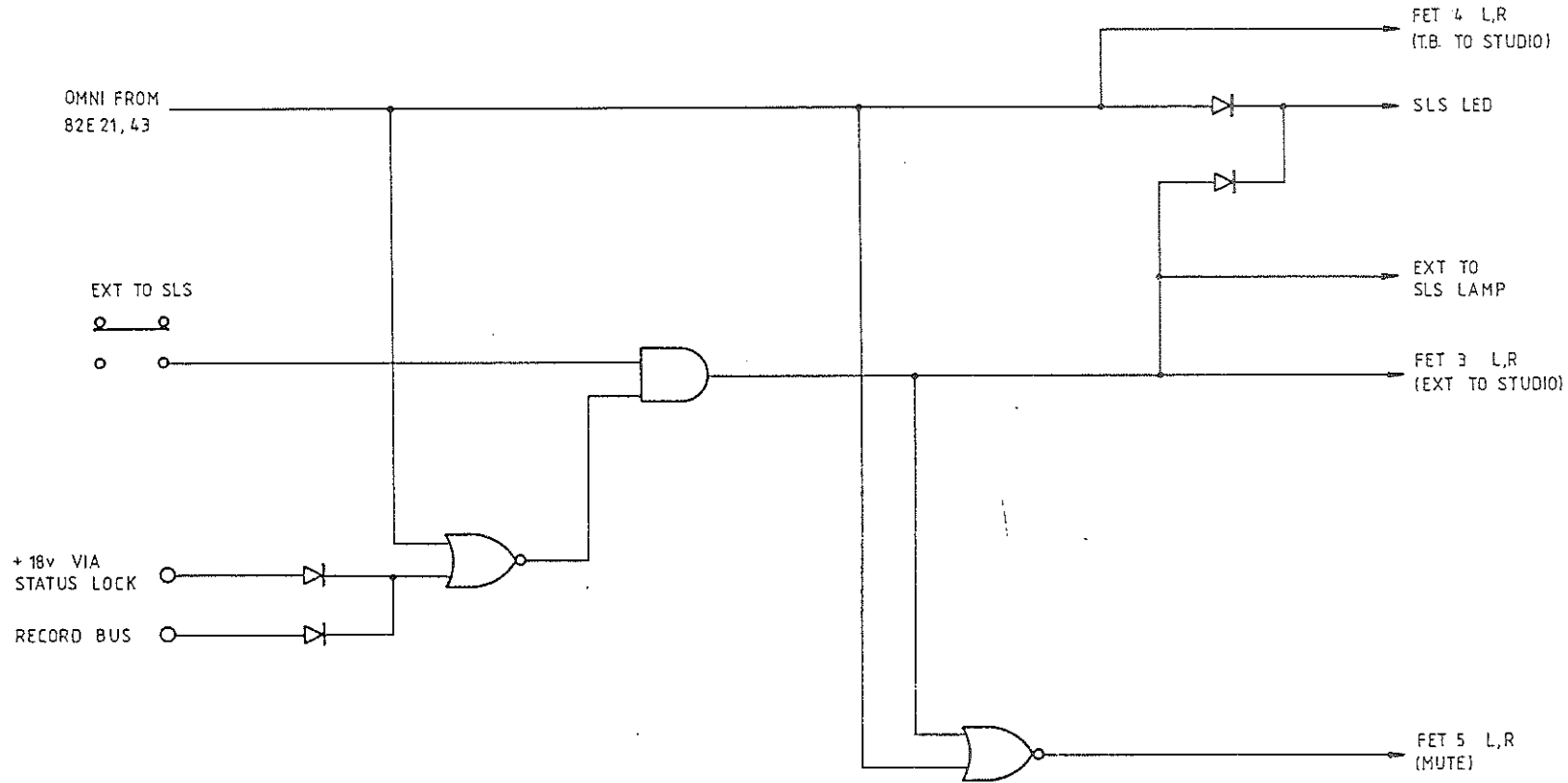
T82E23 55 Way Modulo Connector			
From: EXTERNAL MON BUFFERS & MATRIX. AFL MIX AMP. SLS BUFFERS & OUTPUT AMPS. CF82E23 To: MASTER MODULE SL651E			
No	Description	No	Description
1	611 AFL Mix Bus	29	688V AFL Mix Bus R
2	611 AFL Mix Bus Ov	30	AFL Level pot CW (R)
3	Ext Mon Buffer Input RB	31	SLS Output L-
4	Ext Mon Buffer Input LB	32	SLS Output L+
5	Ext Mon Buffer Input RF (R)	33	Status Lock Bus
6	Ext Mon Buffer Input LF (L)	34	Ext to SLS Switch Lamp
7	Ext Mon Buffer Output LF (L)	35	Ext to SLS Switch
8	Quad/Ext to SLS pot CW (L) (Japan)	36	TB to Studio L
9	Quad/Ext to SLS pot CW (R) (Japan)	37	SLS Level pot Wiper L
10	AFL Level pot CW (L)	38	688V AFL Mix Bus Ov
11	Quad to Studio Switch (Japan)	39	688V AFL Mix Bus L
12	Ext Mon Buffer Output RF (R)	40	No pin
13	Keyway	41	No pin
14	Quad to Studio L (Japan)	42	No pin
15	Quad to Studio R (Japan)	43	No pin
16	Ext Mon Buffer Output LB	44	No pin
17	Ext Mon Buffer Output RB	45	Omni Switch (from 82E21, 43)
18	Record Status Bus	46	611 AFL Enable
19	Ext to SLS L	47	SLS On Indicator (via 82E237)
20	SLS Level pot CW L	48	+11v
21	Ext to SLS R	49	+18v
22	SLS Level pot CW R	50	No pin
23	Echo Return AFL L	51	-18v
24	Echo Return AFL R	52	No pin
25	SLS Output R-	53	0v
26	SLS Output R+	54	0v
27	SLS Level pot Wiper R	55	0v
28	TB to Studio R		

T82023.51
9 June 87

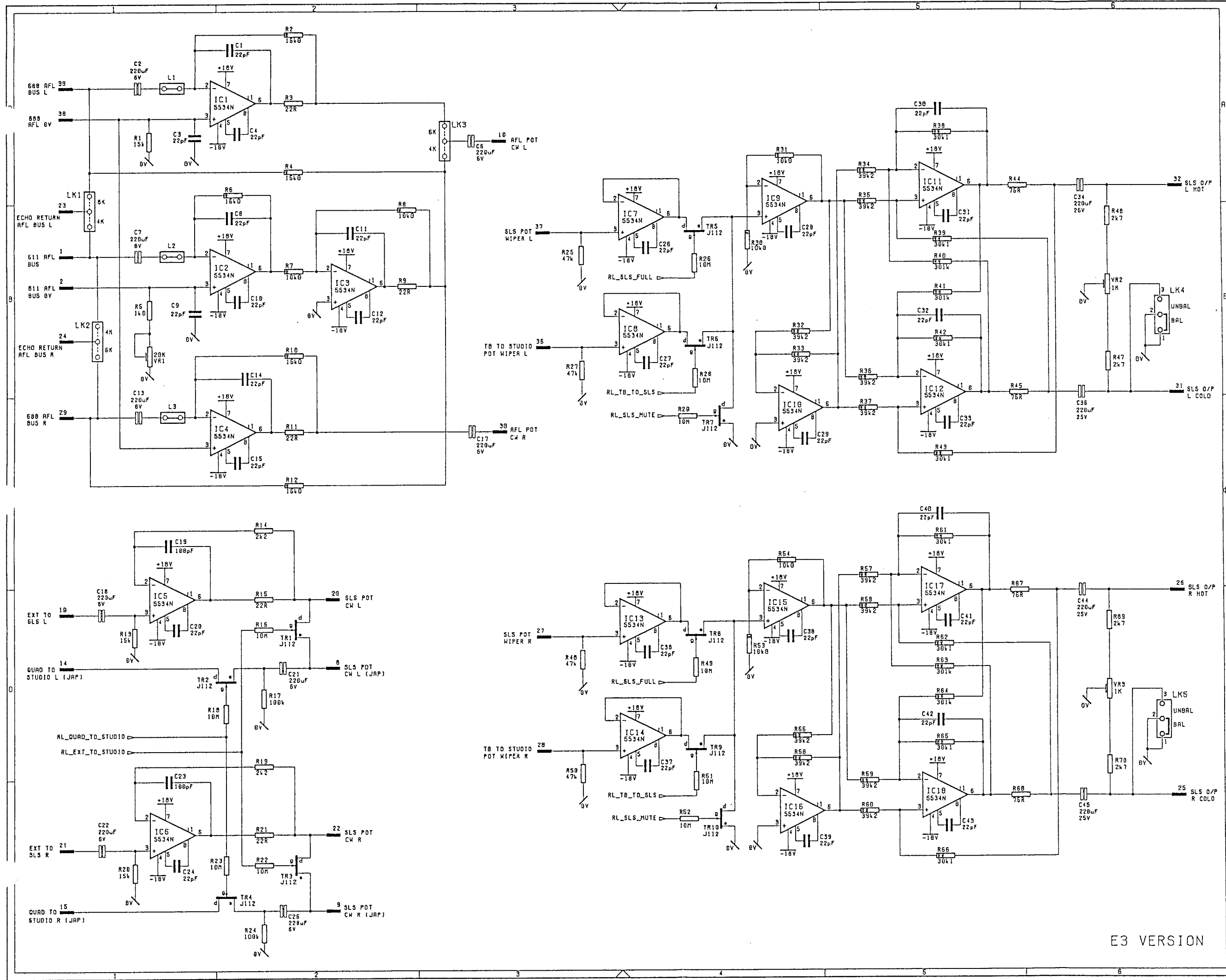
TRAINING 08

Copyright © SSL All rights reserved.
This document may not be reproduced in any form without the written permission of SSL

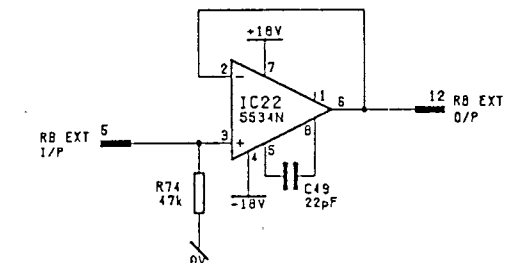
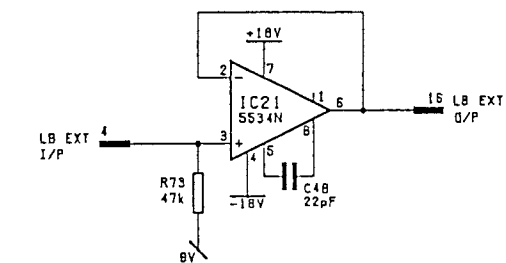
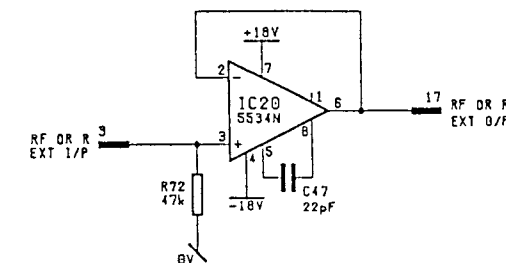
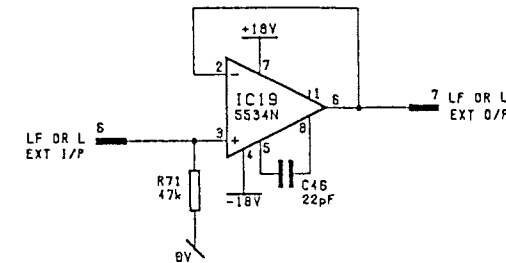
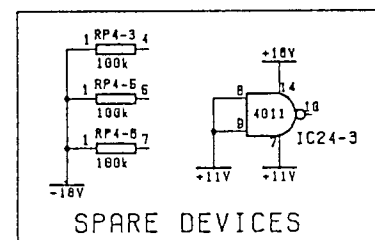
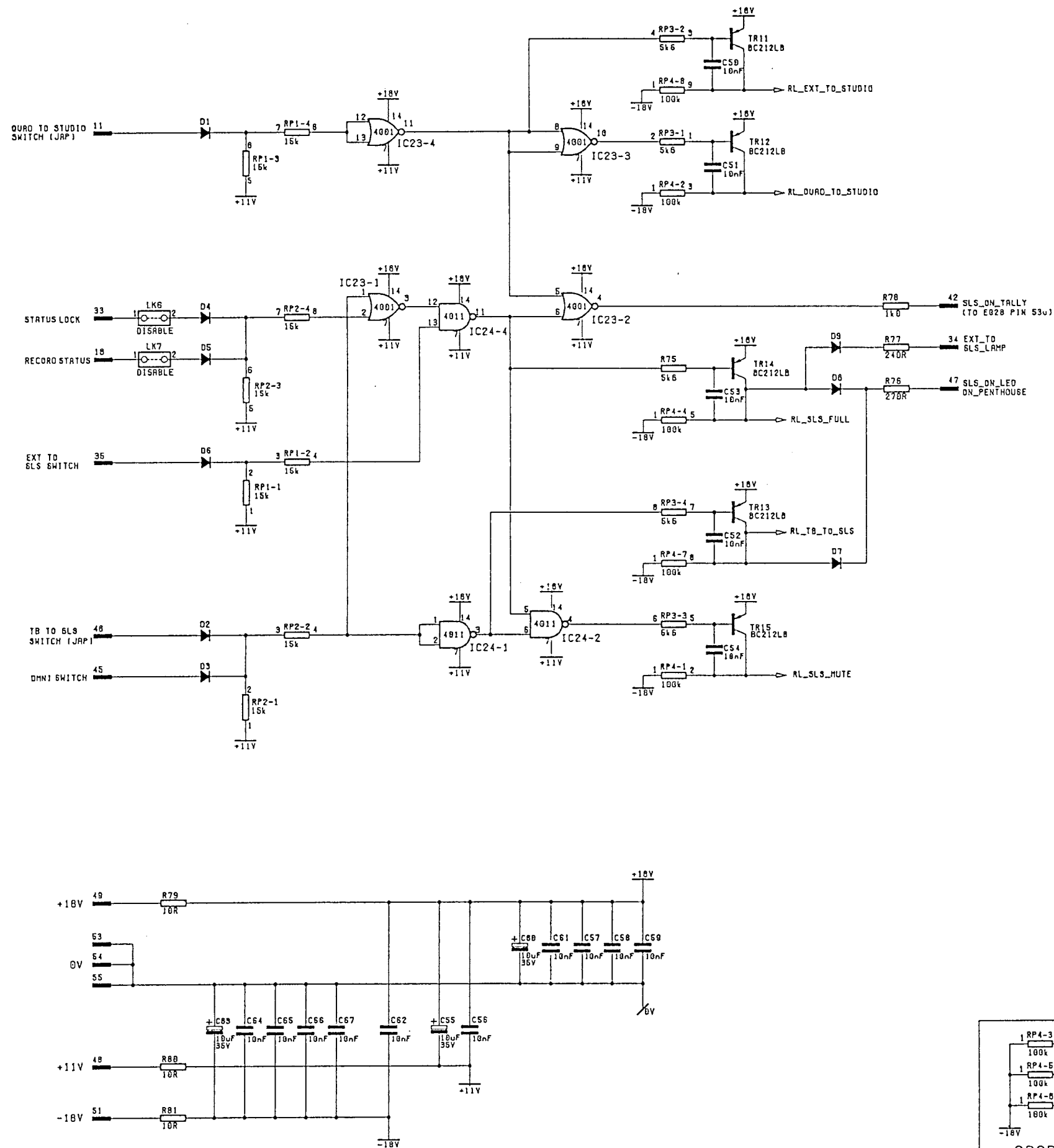
Rev.	Date	Details
1	5.85	REDRAWN V.B.
2	Jan 86 etc	FET Nos 25,26,27 NOW 4,3,5



Title	82E 23
	SIMPLIFIED LOGIC
Drg.No.	TRAINING .08
	Solid State Logic
	Stonesfield · Oxford · England



COPYRIGHT © SSL ALL RIGHTS RESERVED. THIS DOCUMENT MAY NOT BE REPRODUCED IN ANY FORM WITHOUT THE WRITTEN PERMISSION OF SOLID STATE LOGIC.				
REV	ISS	DATE	DETAILS	
0	A	6 AUG 90	NEW DRAWING	BC STEFF
1	A	16 OCT 92	ECD 4K/975 C9 WAS 100PF NDW 22PF	MM
PCB ISSUE PR				
USED ON		651G	A2	
TITLE SLS & AFL				
DRG.NO. T82023.71.3				
SHEET 1 OF 2				
Solid State Logic				



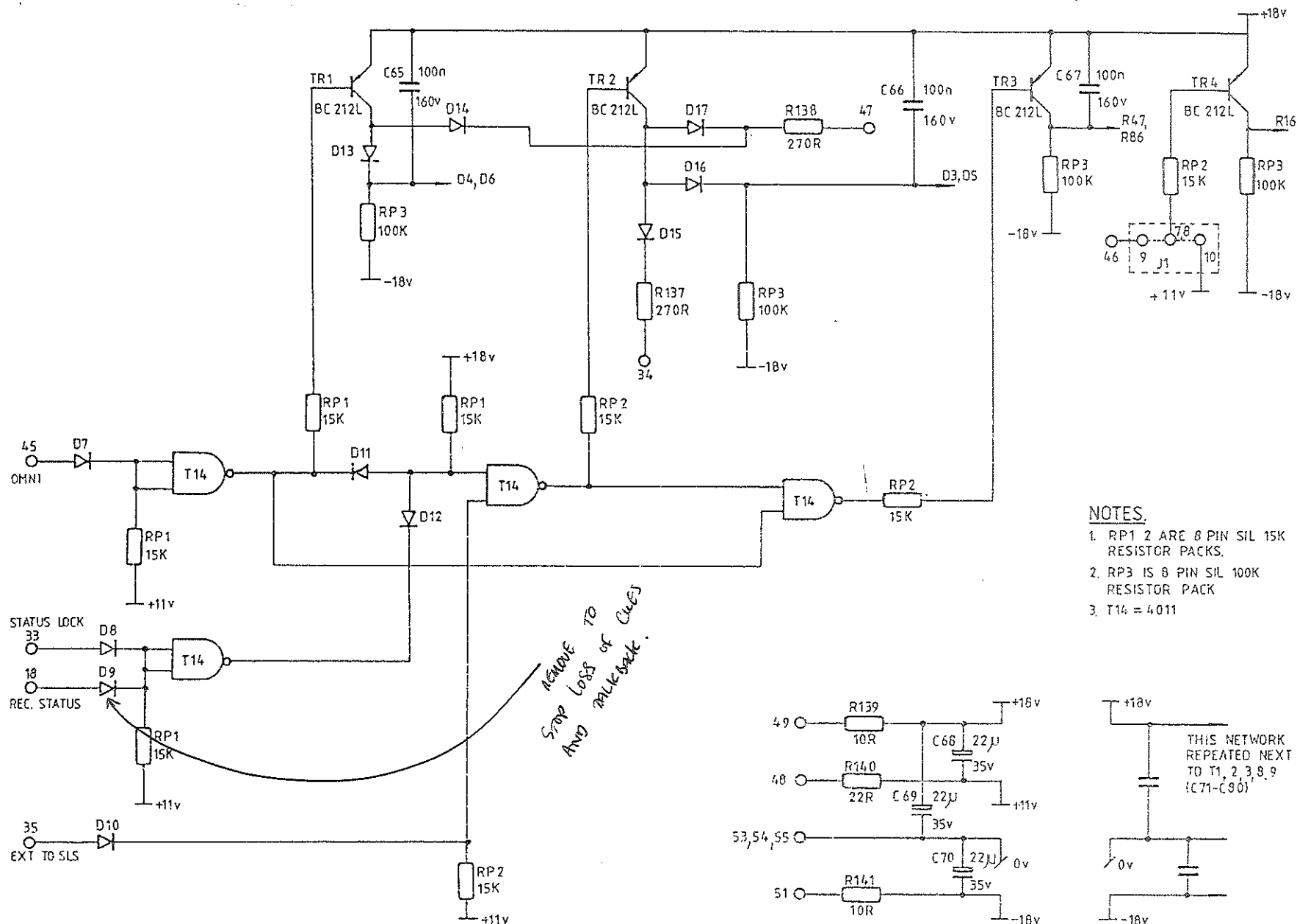
E3 VERSION

COPYRIGHT © SSL ALL RIGHTS RESERVED.
THIS DOCUMENT MAY NOT BE REPRODUCED
IN ANY FORM WITHOUT THE WRITTEN
PERMISSION OF SOLID STATE LOGIC.

REV	ISS	DATE	DETAILS
0	A	3 AUG 50	NEW DRAWING BC STEFF
1	A	16 OCT 52	ECO 4K/975 NO CHANGE MM

PCB ISSUE PR		
USED ON	651G	A2
TITLE SLS & AFL		
ORG. NO. T82023.72.3		
SHEET 2 OF 2		

Solid State Logic



NOTES

1. RP1 2 ARE 8 PIN SIL 15K RESISTOR PACKS.
2. RP3 IS 8 PIN SIL 100K RESISTOR PACK
3. T14 = 4011

Copyright © SSL All rights reserved.
This document may not be reproduced in any form without the written permission of SSL

Rev.	Issue	Ckd	Details
5	a	10-84	REDRAWN V.B.
5	b	5-85	ALL INPUTS PUT
6	a	Feb86	ASSY REV No UPDATED
7	a	Mar86	ASSY REV No UPDATED
7	b	July86	TITLES ADDED TO ECON 18:33:35:45

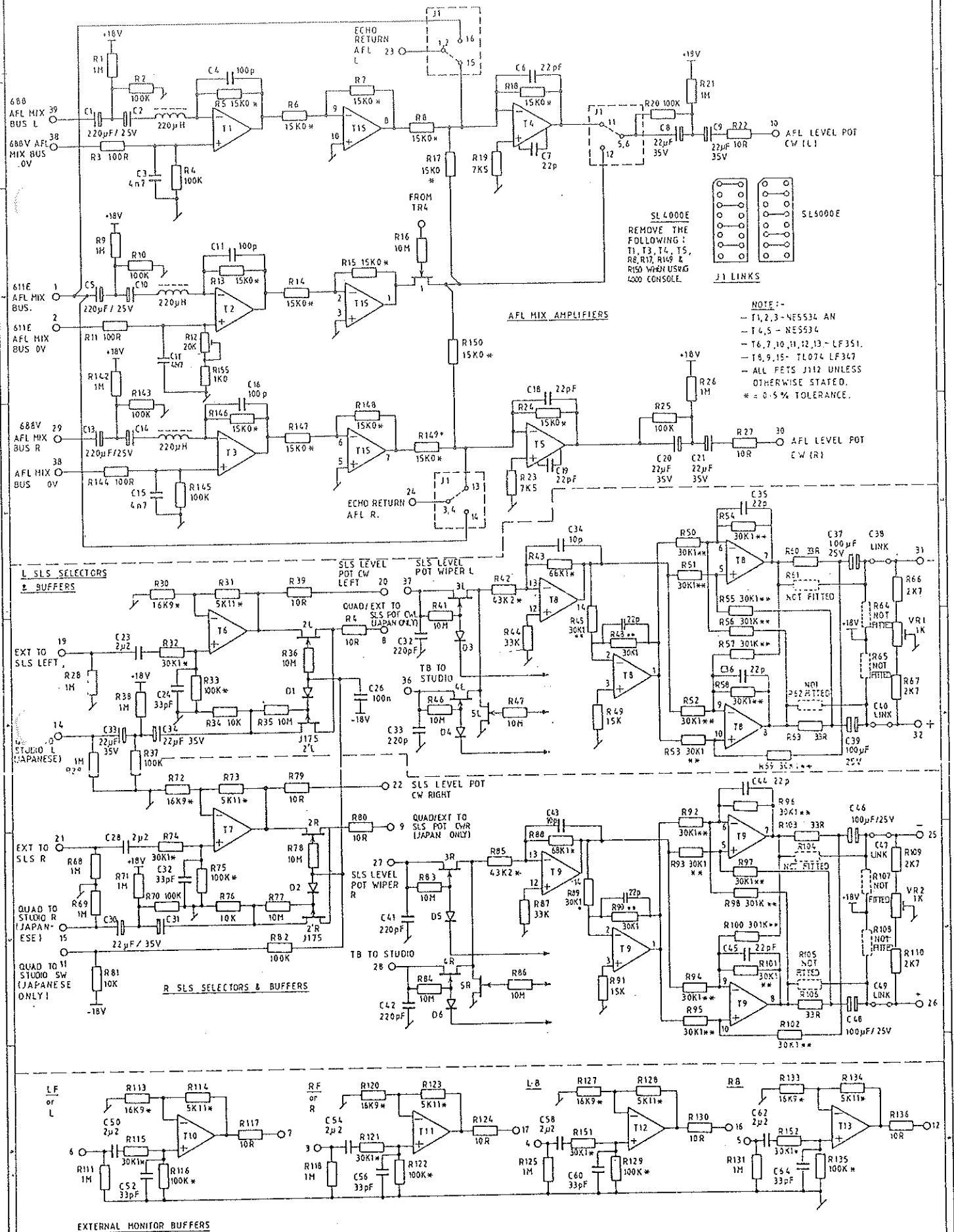
Title 82E23

LOGIC AND POWER

Drg. No. T82023-73

Solid State Logic

Stonesfield · Oxford · England



Rev	Issue	Chgd	Details
1	1	114	REWORKED D.O.
2	2	114	REWORKED D.O.
3	3	114	REWORKED D.O.
4	4	114	REWORKED D.O.
5	5	114	REWORKED D.O.
6	6	114	REWORKED D.O.
7	7	114	REWORKED D.O.
8	8	114	REWORKED D.O.
9	9	114	REWORKED D.O.
10	10	114	REWORKED D.O.
11	11	114	REWORKED D.O.
12	12	114	REWORKED D.O.
13	13	114	REWORKED D.O.